R19

Reg. No:

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR
(AUTONOMOUS)
B.Tech I Year II Semester Supplementary Examinations March-2021
SWITCHING THEORY AND LOGIC DESIGN
(Electronics and Communication Engineering)

Time: 3 hours   Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1   Convert the following to Decimal and then to Octal   **12M**
  i) $(1234)_{16}$
  ii) $(12EF)_{16}$
  iii) $(10110011)_2$
  iv) $(10001111)_2$
  v) $(352)_{10}$
  vi) $(999)_{10}$

OR

2   Simplify the following Boolean expression:
 a $F = (A+B)(A'+C)(B+C)$.   **6M**
 b $F = A+B+C'+D(E+F)$ **6M**

UNIT-II

3   **a**   Minimize the following Boolean function using K-Map   **6M**
  $F(A, B, C, D)= \Sigma m(0, 2, 4, 6, 8, 10, 12, 14)$.
 b Realize it using NAND Gates.   **6M**

OR

4   Simplify the following Boolean function using Tabulation method   **12M**
 $Y(A,B,C,D) = \Sigma(1,3,5,8,9,11,15)$

UNIT-III

5   What is encoder? Design octal to binary encoder.   **12M**

OR

6   **a** Implement the following Boolean function using 8:1 multiplexer.   **5M**
  $F(A,B,C,D) = A'BD'+ACD+B'CD+A'C'D$.
 b What is multiplexer? Construct 4*1 multiplexer with logic gates and truth table.   **7M**

UNIT-IV

7   **a** Design D Flip Flop by using SR Flip Flop and draw the timing diagram.   **6M**
 b Write the differences between combinational and sequential circuits.   **6M**

OR

8   Design a binary counter having repeated binary sequence using JK flip flops: 0,1,2,4,5,6.   **12M**

UNIT-V

9   Explain the minimization procedure for determining the set of equivalent state of a   **12M**
specified machine M.

OR

10   Given the 8-bit data word 01011011, generate the 12-bit composite word for the   **12M**
hamming code that corrects and detects single errors.

*** END ***